AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-4 Cancelled

5. (Currently Amended) A data bus for a plurality of nodes which exchange data with one another over at least one electrical line, said data bus comprising:

a plurality of data exchange modules each having a first input for receiving input data from respective ones of said plurality of nodes and providing a corresponding electrical output signal;

a logic decision gate having a plurality of inputs with each input receiving said respective electrical output signal wherein a single output of said decision gate is connected to a second input of each of said plurality of data exchange modules; and

a signal preparation circuit positioned between said logic decision gate and said second input of said data exchange modules wherein said signal preparation circuit includes means for adjusting the output signal of said logic decision gate to a pulse form.

6. (Previously Presented) The data bus according to claim 5, wherein each of said data exchange modules comprises an opto-electrical transducer wherein an output of said nodes is connected through an optical transmission element to said opto- electrical transducer.

7. (Cancelled)

8. (Currently Amended) The data bus according to claim ~~7~~ 5, further comprising additional logic decision gates positioned between an output of said signal preparation circuit and one of said nodes.

9. (Currently Amended) An improved method of exchanging data among a plurality of nodes, comprising the steps of:

providing a logical decision gate having a plurality of inputs corresponding to the number of plurality of nodes;

outputting information from each of said plurality of nodes;

converting said information into perspective electrical outputs;

providing said electrical outputs to said inputs of said logical decision gate; and providing an output of said logical decision gate transforming said output and providing said transformed output to an input of each of said nodes; and

providing a signal preparation circuit between said logic decision gate output and said plurality of nodes in order to provide a pulse formation adjustment of said output signal.

10. (Cancelled)